IBM Chip Design System: The Big Picture Model

IBM Blue Logic™ Chip Design System: Methodology, Tools, IP, and Services

IBM Chip Design Subprocesses

1. Design Entry and Analysis
   - Technology-independent (exceptions are large macros and complex cores)
   - Technology-dependent

2. Technology Optimization
   - Technology-dependent

3. Design Verification
   - Technology-dependent

4. Layout (Physical Design)
   - Technology-dependent

Chip design specification
Architecture planning and development
- Design partitioning

Translation of functional specification into the HDL View
Analysis of the HDL View of specification

Logic synthesis into gate-level Netlist View
Test structures inspection (design-for-test) synthesis
Clock planning and insertion
Preparation for floorplanning II and placement
Floorplanning II and placement

Functional verification by formal methods
Test structure verification (DFT structures)
Timing verification of specification performance
Power estimation
Prelayout technology checks

Floorplanning III and placement
Pace and route
Timing back-annotation (RC and CAP files, SDF)
Static timing analysis
Post-layout technology checks

Release to mask (reticle) Netlist
Automated test pattern generation (ATPG)

Padframe system (image)
User Netlist import and sanity check
IBM synthesis library

Floorplanning subprocess “straddle”

IBM simulation library

User timing assertions

Data Languages for Design System Communications

IBM supported Merchant Tools

Source: 2004 Chip Design Factory™ Study